IN THE CLAIMS:

Claims 1-23 (cancelled)

Claim 24 (new) A integrated circuit comprising:

a. a lateral NPN transistor having an emitter electrode, a base electrode, and a collector electrode, the NPN transistor operable to conduct current between the emitter electrode and the collector electrode upon a first positive avalanche voltage applied between the emitter electrode and collector electrode;

b. an input element operable to receive a input voltage;

c. a circuitry connected to the input element and to the NPN transistor;

d. an NMOS transistor, having a source electrode, a drain electrode, and a gate electrode, coupled to the lateral NPN transistor;

e. the gate electrode capacitively coupled to input element and resistively coupled to a ground to maintain a voltage corresponding to the input voltage;

f. the NMOS operable to conduct a drain current upon an electrostatic-discharge voltage less positive than the first avalanche voltage applied to the input element, the electrostatic-discharge voltage being more positive than the ordinary operating voltage of the circuitry coupled to the input element;

g. a lateral PNP transistor, having an emitter electrode, a base electrode, and a collector electrode, connected to the input element and resistively coupled to the ground; and

h. the lateral PNP transistor operable to conduct a collector current upon an electrostatic-discharge voltage less positive than the first avalanche voltage applied to the input element, the electrostatic-discharge voltage being more positive than the ordinary operating voltage of the circuitry coupled to the input element, the collector current setting a base voltage at the base electrode of the lateral NPN transistor.